This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims

1. (Previously presented) A method of manufacturing a high density circuit carrier, said method comprising the following method steps:

a) Providing a printed circuit board having circuit traces on at least one side thereof;

b) Coating the circuit board on the at least one side thereof with a dielectric to form a dielectric layer over the circuit traces;

c) Structuring the dielectric layer for producing trenches and vias therein using laser ablation, the trenches not extending completely through the dielectric layer to the circuit traces and the vias extending through the dielectric layer to the circuit traces;

d) Depositing a primer layer onto the entire surface of the dielectric layer or depositing the primer layer into the produced trenches and vias only;

e) Depositing a metal layer onto the primer layer, with the trenches and vias being completely filled with metal for forming conductor structures therein; and

f) Removing the metal layer and the primer layer, except for in the trenches and vias, to expose the dielectric layer if the primer layer has been deposited onto the entire surface in method step d).

2. (Original) The method according to claim 1, characterized in that the trenches and vias are produced in one single process operation in method step c).

3. (Previously presented) The method according to claim 1, characterized in that the trenches and vias are produced using a direct-write technique in method step c).

4. (Previously presented) The method according to claim 3, characterized in that the direct-write technique comprises scanning a laser beam across the dielectric layer at those surface regions of the dielectric layer in which the trenches and vias are to be produced.

5. (Previously presented) The method according to claim 3, characterized in that the direct-write technique further comprises adjusting the power of the laser beam to depend on the depth of the trenches and vias to be produced.

6. (Previously presented) The method according to claim 3, characterized in that the direct-write technique further comprises pulsing the laser beam.

7. (Previously presented) The method according to claim 6, characterized in that the direct-write technique further comprises adjusting the energy amount of the laser beam irradiated to a surface area of the dielectric layer to depend on the depth of the trenches and vias to be produced by setting the number of laser pulses being irradiated to said surface area.

8. (Previously presented) The method according to claim 6, characterized in that the direct-write technique further comprises decreasing the energy amount of successive energy pulses being irradiated to a surface area of the dielectric layer.

9. (Previously presented) The method according to claim 1, characterized in that the trenches and vias are connected to each other in a landless design.

10. (Previously presented) The method according to claim 1, characterized in that the following further method steps are performed once or several times after method step f): g) Depositing another dielectric layer onto the dielectric layer being provided with trenches and vias; and h) Repeating the steps c) through f).

11. (Previously presented) The method according to claim 10, characterized in that a terminating layer is deposited after any one of method steps f) or h).

12. (Previously presented) The method according to claim 1, characterized in that the primer layer is deposited by performing a treatment with metal activators or with monomer solutions for forming conductive polymer layers or with carbon suspensions or by sputtering or performing by a direct deposition method.

13. (Previously presented) The method according to claim 1, characterized in that the metal layer is formed by electroless and/or by electrolytic plating.

14. (Previously presented) The method according to claim 1, characterized in that the metal layer and the primer layer are removed by polishing and/or by a chemical back-etching technique and/or an electrochemical back-etching technique and/or by electropolishing.

15. (Previously presented) The method according to claim 1, characterized in that producing trenches and vias in the dielectric layer in method step c) comprises producing trenches, said trenches also comprising vias.

16. (Previously presented) The method according to claim 1, characterized in that functional layers are deposited onto the metal layer for electrically contacting electric components.

17. (Previously presented) The method of claim 1 wherein the circuit carrier is manufactured in a horizontal line.

18. (Previously presented) The method according to claim 4, characterized in that the direct-write technique further comprises adjusting the power of the laser beam to depend on the depth of the trenches and vias to be produced.

19. (Previously presented) The method according to claim 1, characterized in that a terminating layer is deposited after method step f).

20. (Previously presented) The method according to claim 1, characterized in that the trenches and vias are produced using a direct-write technique in one single process operation in method step c).

21. (Previously presented) The method according to claim 1, characterized in that the printed circuit board is a multilayer circuit board comprising two sides and a conductor pattern on each side.

22. (Previously presented) The method according to claim 7, characterized in that the direct-write technique further comprises decreasing the energy amount of successive energy pulses being irradiated to a surface area of the dielectric.

23. (New) The method according to claim 1 characterized in that the trenches and vias have a V-shape cross-section.

24. (New) The method according to claim 1 characterized in that in method step c) the laser ablation comprises contacting the dielectric layer with a reactive gas during the laser ablation.